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[SEMICONDUCTOR PACKAGE MODULE AND MANUFACTURING MEHOD THEREOF]

Abstract

A process for fabricating a multi-chip package module is disclosed. A substrate, at least a first chip and at least a second chip are provided. The backside of the first chip is attached to a die pad on a substrate. A wire-bonding operation is carried out to electrically connect the first chip and the substrate through conductive wires. A plurality of bumps is bonded to the second chip so that one end of each bump is bonded to a contact on the second chip. Thereafter, the other end of each bump is bonded to a contact on the substrate so that the second chip and the substrate are physically and electrically connected together. Finally, an encapsulation process is performed to form a packaging material enclosing the first chip, the second chip, the conductive wires, the bumps and the substrate.